Patent claims

1. A power-saving multibit delta-sigma converter (1) comprising:

(a) an input (2) for an analog input signal (ZA) and an output (3) for a digital output signal (ZD);

(b) a digital-to-analog converter (4) having a bit width N and serving to convert the digital output signal (ZD) to an analog feedback signal (Z3);

(c) a summing device (5) for forming the difference between the input signal (ZA) and the feedback signal (Z3);

(d) a filter (6) for filtering the difference signal (Z1); and

(e) a clocked quantizing device (7) for quantizing the filtered difference signal (Z2) to form the digital output signal (ZD) with the bit width N;

the quantizing device (7) having fewer than 2^N-1 comparators (21, 22, 23) which compare the filtered signal (22) with a respective reference potential (U0, ... U6) associated with the respective comparator (21, 22, 23) and which each output a comparison result (V1, V2, V3) to a decoder (33), which generates the digital output signal (ZD) from the comparison results (V1, V2, V3),
and the reference potentials (U0, ... U6) being tracked in a manner dependent on a previous comparison result.

2. The multibit delta-sigma converter (1) as claimed in claim 1, characterized
in that the summing device (6) has a differential amplifier (35) for amplifying the difference between the input signal (ZA) and the feedback signal (Z3).

3. The multibit delta-sigma converter (1) as claimed in claim 2, characterized
in that the filter (6) has an integrator for integrating the amplified difference signal (Z1).

4. The multibit delta-sigma converter (1) as claimed in one of the preceding claims,
characterized
in that the quantizing device (7) has a switching controller (8, 12), which switches reference potentials (U0, ... U6) to the comparators (21, 22, 23) in a manner dependent on the previous comparison result, so that at least one of the comparators (21, 22, 23) changes its comparison result (V1, V2, V3) in the event of a change in the input signal (ZA).

5. The multibit delta-sigma converter (1) as claimed in one of the preceding claims,
characterized
in that provision is made of a memory (13) for buffer-storing the digital output signal (ZD).

6. The multibit delta-sigma converter (1) as claimed in one of the preceding claims,
characterized
in that the switching controller (8, 12) is coupled to the memory (13) and switches the reference potentials (U0, ... U6) to the comparators (21, 22, 23) in a manner dependent on the buffer-stored output signal (ZD).

7. The multibit delta-sigma converter (1) as claimed in one of the preceding claims,
characterized
in that the quantizing device (7) has at least one first, second and third comparator (21, 22, 23) each having a first and a second input (24-29) and an output (30, 31, 32), the filtered signal (Z2) being applied to the first inputs (24, 25, 26), the outputs (30, 31, 32) each supplying a comparison result (V1, V2, V3) and a first, second and third reference potential (U0, ... U6) being switched to the second inputs (27, 28, 29), the second reference potential lying between the first and third reference potentials and being closest to the potential of the filtered signal (Z2).

8. The multibit delta-sigma converter (1) as claimed in one of the preceding claims,
characterized

in that the reference potentials (U0, ... U6) are equidistant.

9. The multibit delta-sigma converter (1) as claimed in one of the preceding claims,
characterized
in that 2^N-1 different reference potentials (U0, ... U6) can be switched.

10. A power-saving multibit delta-sigma converter (100) comprising:

(a) an input (2) for an analog input signal (ZA) and an output (3) for a digital output signal (ZD);

(b) a digital-to-analog converter (4) having a bit width N and serving to convert the digital output signal (ZD) to an analog feedback signal (Z3);

(c) a summing device (5) for forming the difference between the input signal (ZA) and the feedback signal (Z3);

(d) a filter (6) for filtering the difference signal (Z1); and

(e) a clocked quantizing device (7) for quantizing the filtered difference signal (Z2) to form the digital output signal (ZD) with the bit width N;

the quantizing device (107) applying a potential offset (PO) to the filtered signal and having fewer than 2^N-1 comparators which compare the filtered signal (Z4) to which said potential offset has been applied with a respective reference potential (U0, ... U6) associated with the respective comparator (21, 22, 23) and which each output a comparison result (V1, V2, V3) to a decoder (33), which generates the digital output signal (ZD) from the comparison results,
and the potential offset (PO) being tracked in a manner dependent on a previous comparison result.

11. The multibit delta-sigma converter (100, 300) as claimed in claim 10, characterized
in that a switching controller (108, 112, 312) is provided, which is coupled to the to outputs (130, 131, 132) of the comparators (121, 122, 123), and sets

the potential offset (PO) in a manner dependent on the comparison results (V301, V302, V303).

12. The multibit delta-sigma converter (200, 300) as claimed in one of the preceding claims,
characterized
in that the digital-to-analog converter (204, 304) and the quantizing device (207, 307) can be operated with the bit width N and with a bit width M = ln(Y+1)/ln(2) corresponding to a number Y of comparators (221, 222, 223, 321, 322, 323).

13. The multibit delta-sigma converter (200, 300) as claimed in claim 12,
characterized
in that the digital-to-analog converter (204, 304) and the quantizing device (207, 307) can be changed over between the two bit widths N and M.

14. The multibit delta-sigma converter (200, 300) as claimed in one of the preceding claims,
characterized
in that the switching controller (208, 212, 239, 308, 312, 339) has a counting device (239, 339) for generating a digital mean value signal (X) in 2^N-Y-digit thermometer code in a manner dependent on the comparison results (V201, V202, V203, V301, V302, V303).

15. The multibit delta-sigma converter (200, 300) as claimed in claim 14,
characterized
in that the counting device (239, 339) has an up/down counter.

16. The multibit delta-sigma converter (200, 300) as claimed in one of the preceding claims,
characterized
in that the decoder (33, 133) has an adding device (238, 338) for forming the N-bit-wide output signal (ZD) by combining the comparison results (V201, V202, V203, V301, V302, V303) with the mean value signal (X).

17. The multibit delta-sigma converter (200, 300) as claimed in one of the preceding claims,

characterized
in that the switching controller (208, 212, 239, 308, 312, 339) has a control logic (212, 312) which, in a manner dependent on the comparison results (V201, V202, V203, V301, V302, V303), either switches the comparison results (V201, V202, V203, V301, V302, V303) in Y-digit, M-bit-wide thermometer code as digital output signal (ZD) or switches the comparison results (V201, V202, V203, V301, V302, V303) combined with the mean value signal (X) as digital output signal (ZD) in 2^N-digit, N-bit-wide thermometer code.

18. The multibit delta-sigma converter (300) as claimed in one of the preceding claims 11 - 18,
characterized
in that the switching controller (308, 312, 339, 342) has a reference digital-to-analog converter (342) for generating the offset potential (PO) from the digital mean value signal (X).

19. The multibit delta-sigma converter (400, 500) as claimed in one of the preceding claims,
characterized
in that the quantizing device (407, 507)

- has a compensation analog-to-digital converter (404, 504) for converting the comparison results (V401, V402, V403) into at least one analog compensation signal (ZK, ZK1, ZK2) and

- has an adding device (408, XP, XN) for subtracting the analog compensation signal (ZK, ZK1, ZK2) from the filtered difference signal (Z2).

20. The multibit delta-sigma converter (400, 500) as claimed in claim 19,
characterized
in that the bit width of the compensation analog-to-digital converter (404, 504) corresponds to the number of comparators (21, 22, 23, 521, 522, 523).

21. The multibit delta-sigma converter (400) as claimed in claim 19 or 20,
characterized
in that provision is made of an amplifier (405) for amplifying the analog

compensation signal (ZK) with a compensation factor.